

REMARKS

This Application has been carefully reviewed in light of the Final Action dated April 11, 2005. Applicant respectfully requests reconsideration and favorable action in this Application.

Claims 1 and 6-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Davis in view of Somasundaram, et al. Independent Claims 1 and 11 recite in general the ability to capture information subsequent to the triggering event in a second set of blocks of the memory array without writing over information captured prior to the triggering event in the first set of blocks of the memory array. By contrast, the Davis patent merely discloses the use of a circular buffer that is used to continuously capture data before a triggering event. The Davis patent contemplates the use of the same circular buffer to capture data after a triggering event by delaying a write disable to the circular buffer. Thus, after the triggering event, the Davis patent captures data in the circular buffer previously used for capturing data prior to the triggering event, overwriting any previously captured data. Additionally, the Davis patent does not contemplate partitioning its circular buffer into a first set of blocks that capture information prior to a triggering event and a second set of blocks separate from the first set of blocks for capturing information after a triggering event. The Davis patent uses its circular buffer as a single set of blocks that capture information. In initial operation, whatever is in the circular buffer of the Davis patent is pre-trigger captured information. When a trigger occurs, post-trigger information is captured by writing over the pre-trigger captured information. As a result, the Davis patent fails to disclose the use of separate first and second sets of blocks in a

memory for respectively capturing information prior to and subsequent to a triggering event and also fails to disclose an ability to capture information subsequent to the triggering event without writing over previously captured information prior to the triggering event as provided in the claimed invention. Moreover, the Somasundaram, et al. patent does not include an on-chip trace recorder capable of capturing any information associated with a triggering event. Therefore, Applicant respectfully submits that Claims 1 and 6-15 are patentably distinct from the proposed Davis - Somasundaram, et al. combination.

Claims 2-5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Davis in view of Somasundaram, et al. and further in view of Voith, et al. Independent Claim 1, from which Claims 2-5 depend, has been shown above to be patentably distinct from the proposed Davis - Somasundaram, et al. combination. Moreover, the Voith, et al. patent does not include any additional disclosure combinable with either the Davis or Somasundaram, et al. patents that would be material to patentability of these claims. Additionally, the Voith, et al. and Davis patents would require more than one circular buffer to process more than one triggering event. Thus, the Voith and Davis patents are not capable of capturing information associated with two triggering events within a single memory unit as required in the claimed invention. Therefore, Applicant respectfully submits that Claims 2-5 are patentably distinct from the proposed Davis - Somasundaram, et al. - Voith, et al. combination.

Claims 16-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Davis in view of Somasundaram, et al. and further in view of Microsoft Computer Dictionary. Independent Claim 16 includes a similar limitation as found in

Claims 1 and 11 discussed above and shown to be patentably distinct from the proposed Davis - Somasundaram, et al. combination. Moreover, the Microsoft Computer Dictionary does not include any additional disclosure combinable with either the Davis or Somasundaram, et al. patents that would be material to patentability of these claims. Therefore, Applicant respectfully submits that Claims 16-20 are patentably distinct from the proposed Davis - Somasundaram, et al. - Microsoft Computer Dictionary combination.

This Response to Examiner's Action is necessary to address a current characterization of the prior art asserted by the Examiner in support of the rejections to the claims. This Response to Examiner's Final Action could not have been presented earlier as the Examiner has only now provided the current characterization of the prior art.

CONCLUSION

Applicant has now made an earnest attempt to place the Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicant respectfully requests reconsideration and full allowance of all pending claims.

The Commissioner is hereby authorized to charge any amount required or credit any overpayment to Deposit Account No. 02-0384 of BAKER BOTTS L.L.P.

Respectfully submitted,

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